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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/944,472	08/30/2001	James J. Howarth	4348US (MUEI-0547.00/US)	1559

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EXAMINER	
DIAZ, JOSE R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/944,472	HOWARTH, JAMES J.	
	Examiner	Art Unit	
	José R Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,6-13,20-24,27,29-33,35,36 and 43-46* is/are pending in the application.

4a) Of the above claim(s) *9,20-23,32 and 43-46* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,6-8,10-13,24,27,29-31,33,35 and 36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/19/04; 11/17/03; 9/25/03; 6/2/03*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 19, 2004 has been entered.

Oath/Declaration

The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because: it is not of sufficient quality to permit the identification of the city and state of residence of the inventor.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 8, 10-11, 24, 31, and 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Shewmaker (US Pat. No. 2,752,580).

Regarding claim 1, Shewmaker teaches a method for aligning a semiconductor device package with a carrier substrate for electrical interconnection therebetween, the method comprising: forming at least two channels (17) through the semiconductor device package (13) from a first major surface thereof to a second, opposing major surface thereof (see figs. 1 and 3); providing a major surface of the carrier substrate (21) with at least two alignment features (22) including forming at least two holes the in the carrier substrates each of which are spaced and positioned in respective correspondence to one of the at least two channels (see figs. 1 and 3); placing the semiconductor device package (13) over the carrier substrate (21) with the first major surface of the semiconductor package facing the major surface of the carrier substrate (see fig. 3); and aligning the at least two channels (17) formed in the semiconductor device package with the at least two alignment features (22) of the carrier substrate (see fig. 3); providing at least two pins (16) (see figs. 1 and 3), wherein at least one of the at least two pins (16) includes a mechanical self-locking mechanism (A,B) proximate at least one end thereof (see figure 3 attached hereto, below); placing the at least two pins (16) through the at least two channels (17) and into the at least two holes (22) (see fig. 2); and engaging a portion of at least one of the second major surface of the semiconductor device package and a second, opposing surface of the carrier substrate with the mechanical self-locking mechanism (see fig. 2).

Regarding claims 8 and 31, Shewmaker further teaches affixing the at least two pins (16) to both the semiconductor device package (13) and to the carrier substrate (21) (see fig. 2).

Regarding claim 10, Shewmaker further teaches forming a mechanical self-locking mechanism at a first end (A) and at a second end (B) of the at least one pin (16) (see figure 3 attached hereto, below).

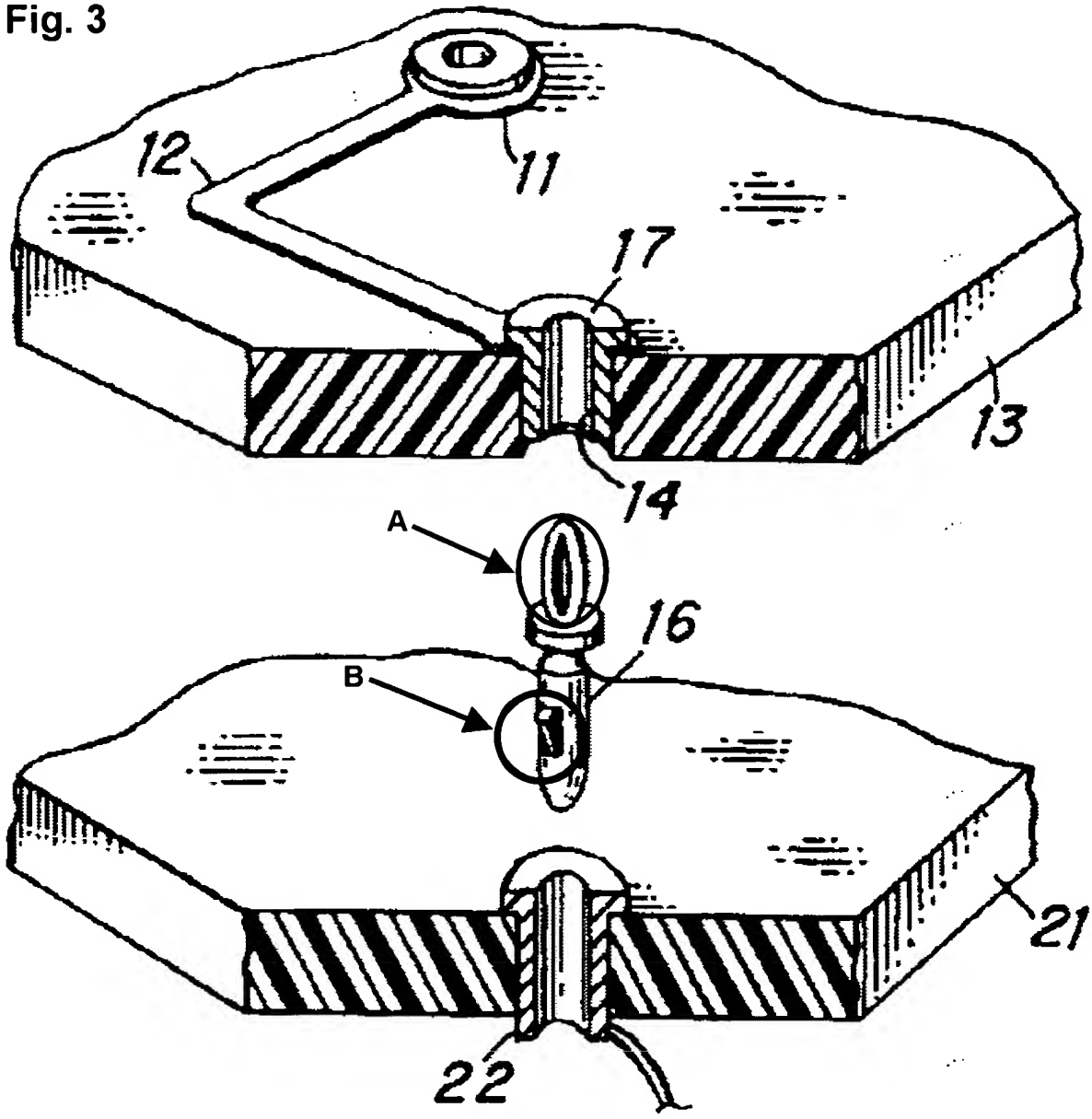
Regarding claim 11, Shewmaker further teaches removing the at least two pins (16) subsequent to the alignment of the at least two channels (17) with the at least two alignment features (22) (see fig. 2 and col. 2, lines 55-58).

Regarding claim 24, Shewmaker teaches a method of testing a semiconductor device package having a plurality of discrete conductive elements disposed in a pattern on a surface thereof, the method comprising: providing a carrier substrate (21) having a plurality of terminal pads (22) arranged in a pattern corresponding to a mirror image of the pattern of discrete conductive elements (see figs. 1 and 3); forming at least two channels (17) in the semiconductor device package (13), each channel passing from a first surface thereof to a second, opposing surface thereof (see figs. 1 and 3); providing the carrier substrate (21) with at least two alignment features including forming at least two holes the in the carrier substrate (consider the hole in which the contact 22 is formed in fig. 3 and col. 2, lines 25-30), each of which are respectively spaced and positioned in correspondence to one of the at least two channels (17) (see figs. 1 and 3); placing the semiconductor device package (13) over the carrier substrate (21) (see fig. 3); aligning each channel of the at least two channels (17) formed in the

semiconductor device package (13) with a corresponding alignment feature of the at least two alignment features (22) of the carrier substrate (21) (see fig. 3) including placing pins (16) through the at least two channels (17) and into the at least two holes (22) (see fig. 2); electrically contacting each discrete conductive element of the plurality with a terminal pad (22) of the plurality (see fig. 2 and col. 3, lines 36-38 and 49-54); and passing at least one electrical signal between the semiconductor device package and the carrier substrate (see col. 2, lines 17-19 and col. 3, lines 36-38 and 49-54); and removing the pins (16) subsequent to the alignment of each of the at least two channels (17) with a corresponding alignment feature of the at least two alignment features (22) (see fig. 2 and col. 2, lines 55-58).

Regarding claim 33, Shewmaker further teaches that forming a mechanical self-locking mechanism (A, B) proximate at least one end of each pin (16) (see figure 3 attached hereto, below).

Fig. 3



Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-7 and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shewmaker (US Pat. No. 2,752,580) in view of Butler et al. (US Pat. No. 5,751,556).

Regarding claims 6-7 and 29-30, Shewmaker fails to teach the limitation of forming the at least two pins of an electrically non-conductive material or of an anti-static material. Butler et al. teaches that it is well known in the art to form the at least two pins (18) of an electrically non-conductive and anti-static material (e.g. plastic) (see col. 5, line 3).

Shewmaker and Butler et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to connect the semiconductor device package and the carrier substrate with plastic pins. The motivation for doing so, as is taught by Butler et al., is to provide a secure connection between the semiconductor device package and the carrier substrate (col. 2, lines 40-41). Therefore, it would have been obvious to combine Butler et al. with Shewmaker to obtain the invention of claims 6-7 and 29-30.

Claims 4, 12-13, 27, 35 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shewmaker (US Pat. No. 2,752,580) in view of Kim (US Pat. No. 5,978,229).

Regarding claims 12-13 and 35-36, Shewmaker teaches the step of aligning the semiconductor device package (13) having the at least two pins (16) inserted through the at least two channels (17) with the carrier substrate (21) having the at least two holes (22) (see fig. 2 and col. 2, lines 48-54).

However, Shewmaker fails to teach the further limitation of using a pick and place device to align the semiconductor device package with the carrier substrate. Kim teaches that it is very well known in the art to use a pick and place device to align the semiconductor device package (10) with the carrier substrate (20) (see fig. 5). Please consider the combination of the holder (30) and the semiconductor device package (10) as the head of the pick and place device (see fig. 5).

Shewmaker and Kim are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to include a pick and place device, wherein the head of the pick and place device comprises a holder, and a semiconductor device package having the at least two pins inserted through the at least two channels. The motivation for doing so, as is taught by Kim, is increasing the efficiency of production of electrical systems (col. 2, lines 40-43). Therefore, it would have been obvious to combine Kim with Shewmaker to obtain the invention of claims 4, 12-13, 27, 35 and 36.

Regarding claims 4 and 27, Kim further teaches placing the pins (50a) into at least two blind holes (54a) (see fig. 10A).

Response to Arguments

Applicant's arguments with respect to claims 1, 4, 6-8, 10-13, 24, 27, 29-31, 33, 35 and 36 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Straus (US Pat. No. 3,568,001) discloses a snap-on pin (see fig. 1); Hopfer et al. (US Pat. No. 5,761,036) discloses mechanically and electrically attaching an IC (12) to a circuit board (10) (see figs. 1, 4 and 5); Matsumura (2001/0046127 A1) discloses an IC (11) having positioning holes (13) (see fig. 4); Miazga (US Pat. No. 5,117,330) discloses fixing a circuit component (22) to a circuit board (28) with clip mechanisms (42, 44) (see figs. 1 and 3); Ignasiak (US Pat. No. 4,841,100) discloses a snap-on pin (see fig. 2); and Hoge (US Pat. No. 5,313,015) discloses a pin (70) (see fig. 3).

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on 9:00-5:00 Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JRD
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